CLAIMS

What is claimed is:

1. A manufacturing process of a nano device transistor for a biosensor, the manufacturing process being used for forming a structure of an off-set nano device transistor, the manufacturing process comprising the following steps:

depositing a bottom gate on a silicon substrate having SiO_2 deposited on it;

depositing a gate dielectric layer to be an interface layer for insulating the bottom gate;

coating a nano channel layer;

depositing a drain and a source on the boundary of the nano channel layer and the gate oxidization layer;

depositing a protection layer and performing coating, lithography and etching to form a first protection layer and a second protection layer, the first protection layer and the second protection layer being used for separately covering

and insulating the drain and the source so as to define an off-set area on the boundary of the first and second protection layers and the nano channel layer; and

performing the lithography wet etching for defining a detection area;

wherein the detection area is used for detecting an object so as to achieve the object of detecting the specific bio species for bio measurement.

2. The manufacturing process of claim 1, wherein the bottom gate is made of the material of metal or poly-silicon.

3. The manufacturing process of claim 1, wherein a surfactant and the anti-body for the object to be detected are absorbed on the refurbished nano channel layer.

4. The manufacturing process of claim 1, wherein the drain and the source are metal electrodes.

5. The manufacturing process of claim 1, wherein the first protection layer and the second protection layer are made of the material of SiO_x, SiN_x or other insulation

materials.

6. The manufacturing process of claim 1, wherein the gate dielectric layer is made of the material of SiO_x, SiN_x or other gate dielectric materials.

7. A manufacturing process of a nano device transistor for a biosensor, the manufacturing process being used for forming a structure of a double gate nano device transistor, the manufacturing process comprising the following steps:

depositing a bottom gate on a silicon substrate having SiO_2 deposited on it;

depositing a gate dielectric layer to be an interface layer for insulating the bottom gate;

coating a nano channel layer;

depositing a drain and a source on the boundary of the nano channel layer and the gate oxidization layer;

depositing a ceiling gate dielectric layer for insulating the drain and the source from the nano channel layer;

depositing a ceiling gate above the ceiling

gate dielectric layer, and performing a lithography etching method to define the shape of the ceiling gate; and

depositing a protection layer and then performing the lithography etching method to make the ceiling gate dielectric layer etched downward so as to form a first ceiling gate dielectric layer and a second ceiling gate dielectric layer, and the two-sides separated ceiling gate dielectric layer being covered with a first protection layer and a second protection layer so as to define and form a detection area;

wherein the detection area is used for detecting an object so as to achieve the object of detecting the specific bio species for bio measurement.

8. The manufacturing process of claim 7, wherein the bottom gate is made of the material of metal or poly-silicon.

9. The manufacturing process of claim 7, wherein a surfactant and the anti-body for the object to be detected are absorbed on

the refurbished nano channel layer.

10. The manufacturing process of claim 7, wherein the drain and the source are metal electrodes.

11. The manufacturing process of claim 7, wherein the first protection layer and the second protection layer are made of the material of SiO_x, SiN_x or other insulation materials.

12. The manufacturing process of claim 7, wherein the gate dielectric layer is made of the material of SiO_x, SiN_x or other gate dielectric materials.

13. The manufacturing process of claim 7, wherein the ceiling gate is made of the material of metal.

14. The manufacturing process of claim 7, wherein the first ceiling gate dielectric layer and the second ceiling gate dielectric layer are made of the material of SiO_x, SiN_x or other gate dielectric materials.

15. The manufacturing process of claim 7, wherein the position of the ceiling gate is any position on the ceiling gate

dielectric layer, and the ceiling gate covers a portion of the nano channel layer.

16. A structure of a nano device transistor for a biosensor, a detection area of an off-set nano device transistor being used for detecting an object so as to detect the specific bio species, the structure comprising:

a silicon substrate having SiO_2 deposited on it;

a bottom gate positioned on the silicon substrate having SiO_2 deposited on it;

a gate dielectric layer being an interface layer for insulating the bottom gate;

a nano channel layer positioned on the gate dielectric layer;

a drain positioned on the boundary of the nano channel layer and the gate dielectric layer;

a source positioned on the boundary of the nano channel layer and the gate dielectric layer;

a first protection layer for covering and insulating the drain; and

a second protection layer for covering and insulating the source;

wherein by means of the first protection layer, the second protection layer and the nano channel layer, a detection area is defined, and then used for detecting an object to be detected so as to achieve the object of detecting the specific bio species for bio measurement.

17. The structure of claim 16, wherein the bottom gate is made of the material of metal or poly-silicon.

18. The structure of claim 16, wherein a surfactant and the anti-body for the object to be detected are absorbed on the refurbished nano channel layer.

19. The structure of claim 16, wherein the drain and the source are metal electrodes.

20. The structure of claim 16, wherein the first protection layer and the second protection layer are made of the material of SiO_x, SiN_x or other insulation materials.

21. The structure of claim 16, wherein the gate dielectric layer is made of the

material of SiO_x, SiN_x or other gate dielectric materials.

22. The structure of claim 16, wherein the first protection layer, the second protection layer and the nano channel layer are used for defining a detection area.

23. The structure of claim 16, wherein a plurality of off-set nano device transistors are connected to form a serial connection structure of the off-set nano device transistors.

24. The structure of claim 16, wherein a plurality of nano channel layers are connected between the drain and the source in the structure of the off-set nano device transistor, or a plurality of off-set nano device transistors are connected so as to form a parallel connection structure of the off-set nano device transistor.

25. A structure of a nano device transistor for a biosensor, a detection area of a double gate nano device transistor being used for detecting an object so as to detect the specific bio species, the structure

comprising:

a silicon substrate having SiO_2 deposited on it;

a bottom gate positioned on the silicon substrate having SiO_2 deposited on it;

a gate dielectric layer being an interface layer for insulating the bottom gate;

a nano channel layer positioned on the gate dielectric layer;

a drain positioned on the boundary of the nano channel layer and the gate dielectric layer;

a source positioned on the boundary of the nano channel layer and the gate dielectric layer;

a ceiling gate dielectric layer positioned on the drain and the source, comprising a first ceiling gate dielectric layer and a second ceiling gate dielectric layer;

a ceiling gate positioned on the ceiling gate dielectric layer;

a first protection layer positioned on the surface of the first ceiling gate

dielectric layer;

a second protection layer positioned on the surface of the second ceiling gate dielectric layer;

wherein the first protection layer, the second protection layer, and the first ceiling gate dielectric layer, the second ceiling gate dielectric layer and the nano channel layer are used to define a detection area for detecting an object so as to achieve the object of detecting the specific bio species for bio measurement.

26. The structure of claim 25, wherein the bottom gate is made of the material of metal or poly-silicon.

27. The structure of claim 25, wherein a surfactant and the anti-body for the object to be detected are absorbed on the refurbished nano channel layer.

28. The structure of claim 25, wherein the drain and the source are metal electrodes.

29. The structure of claim 25, wherein the first protection layer and the second protection layer are made of the material

of SiO_x, SiN_x or other insulation materials.

30. The structure of claim 25, wherein the gate dielectric layer is made of the material of SiO_x, SiN_x or other gate dielectric materials.

31. The structure of claim 25, wherein the ceiling gate is made of the material of metal.

32. The structure of claim 25, wherein the first ceiling gate dielectric layer and the second ceiling gate dielectric layer are made of the material of SiO_x, SiN_x or other insulation materials.

33. The structure of claim 25, wherein the position of the ceiling gate is any position on the ceiling gate dielectric layer, and the ceiling gate covers a portion of the nano channel layer.

34. The structure of claim 25, wherein a plurality of double gate nano device transistors are connected to form a serial connection structure of the double gate nano device transistors.

35. The structure of claim 25, wherein a

plurality of nano channel layers are connected between the drain and the source in the structure of the double gate nano device transistor, or a plurality of double gate nano device transistors are connected so as to form a parallel connection structure for the double gate nano device transistor.